Annual Report

for

Office of Naval Research

Contract Number: N00014-96-1-0771

for a program of research entitled:

Sub-Micron Lithography with the Atomic Force Microscope

Reporting Period: January 1, 1997 through December 31, 1997

4-8-98

Principal Investigator
Calvin F. Quate
Leland T. Edwards Research Professor
Edward L. Ginzton Laboratory
Stanford University
Stanford, CA 94305-4085
Telephone: (650) 723-0213
Fax: (650) 725-2189
E-mail: quate@ee.stanford.edu

Progress Report for 1997 -- DARPA/ULTRA

I - Introduction

This was a year or progress where we consolidated our gains with parallel arrays of cantilevers, fabricating operating devices (pMOSFETs) using scanning probes as the lithography tool and for in-depth studies of the response of E-beam resist when exposed with electrons from the scanning tips. Our report is divided as follows:

High speed atomic force microcopy with parallel arrays of cantilevers
Fabrication of pMOSFET's with SPL Lithography
Lithography with Hybrid AFM/STM Probes

II -High speed atomic force microcopy with parallel arrays of cantilevers

An expandable system has been developed to operate multiple probes for the atomic force microscope (AFM) in parallel at high speeds. The combined improvements from parallelism and enhanced tip speed in this system represent an increase in throughput by over two orders of magnitude. A modular cantilever design has been replicated to produce an array of 50cantilevers with a 200 μm pitch. This design contains a dedicated integrated sensor and integrated actuator where the cells can be repeated indefinitely. Electrical shielding within the array virtually eliminates coupling between the actuators and sensors. The reduced coupling simplifies the control electronics facilitating the design of a computer system to automate the parallel high speed arrays. This automated system has been applied to four cantilevers within the array of 50 cantilevers, with a 20kHz bandwidth and a noise level of less than 50Å. For typical samples, this bandwidth allows us to scan the probes at 4mm/s.

As the semiconductor industry continues to shrink its design rules, new advanced metrology and lithography tools become increasingly important. There has been much recent work on applying the well known techniques of scanning probe microscopy (SPM) to these problems. The crux of these efforts is to maintain the resolution and precision of the probe based system while increasing its capacity, in terms of area scanned in a given time, to a level that is viable for commercial purposes. The throughput of the scanning probe microscope system has been enhanced by moving to parallel operation with arrays, and by increasing the scanning speed of each probe.

The parallel system is a direct approach to increasing the speed of the SPM system since the throughput of a microscope is increased in direct proportion to the number of tips in an array. Integrating deflection, or force, sensors onto the cantilever simplifies the operation of the parallel system because it reduces the necessary alignment and maintenance required for operation. The piezoresistive AFM sensor, developed by Tortonese[1] et al., has been incorporated into parallel arrays and has been used for imaging and lithography[2]. Many other groups have adopted the piezoresistive sensor for probe systems. Parallel piezoresistive cantilevers for data storage applications have been fabricated by Chui[3] et al. and Ried[4] et al. Parallel optical lever cantilever sensors have been demonstrated by Lang[5] et. al. for use in imaging and other sensing applications.

In most probe systems, throughput is limited by the speed at which the tip can be scanned over the sample surface. For constant force imaging this speed is generally limited by the speed of

the feedback system which is in turn limited by the speed, or resonance, of the z-axis actuator. High speed imaging has been previously done by Barrett[6] et al. and Mamin[7] et al. These systems serve as powerful demonstrations but they are not total solutions. Barrett's system operated in a non-feedback mode and thus required hard samples. Mamin's system scanned the sample with a low displacement high resonance actuator and thus limited the mass and topography of the sample. Manalis[89] et al. has used both piezoresistive and optical sensing on cantilevers with integrated actuators for high speed imaging.

Our automated cantilever array design allows parallel constant force imaging at high speeds. The footprint of the cantilever structure has been modified to occupy a slice only 200μm in width, allowing the devices to be placed in a 1-D expandable parallel array. Improved electrical performance of the device allows us to use minimal non-synchronous electronics, permitting simple fabrication of the control system onto a personal computer (PC) expansion card. The integrated electronics, coupled with the PC control, provides automated operation over the array.

We have shown that the scan speed of the AFM could be increased by an order of magnitude over the standard AFM by integrating a thin layer of ZnO on the base of a piezoresistive cantilever. The voltage applied to the ZnO film bends the cantilever to conform to the sample topography and thus maintain constant force on the tip. The sample force was detected by measuring resistance changes in the piezoresistor. In that study, electrical coupling between the ZnO actuator and the piezoresistive sensor required the use of a synchronous system. Although this technique significantly increased the imaging speed, unwanted capacitance in the detection circuitry limited the bandwidth to 6 kHz. Ideally, the imaging bandwidth should be limited by the mechanical resonance of the cantilever when the tip is in contact with a surface. Ultimately the design must have the versatility to control an electrical interaction between the tip and sample (for lithography, modification, etc.). Therefore a provision to bias the tip without interfering with the sensing and actuating properties of the device must be included in the design.
Our new cantilever, designed to address these issues, is schematically shown along with a brief process flow in Fig. 1. Inspection of this figure reveals several key features in the new design. First, the bottom electrode of the actuator (between the ZnO and the silicon substrate) serves as a grounding plane. This prevents the signals that are applied to the top ZnO electrode from coupling capacitively to the piezoresistor through the silicon substrate. Second, the piezoresistor is defined by a patterned implant and this allows the cantilever to be actuated with a single pad of ZnO. In the previous design, the piezoresistor was defined by physical etching thereby requiring the ZnO to be patterned on both of the cantilever legs. We found that the dual leg ZnO configuration reduced the overall yield of working devices. Third, grounding busses are added for common piezoresistor and common ZnO electrodes. This minimized the tip to tip spacing by eliminating two electrical contacts per cantilever. Finally, a dedicated voltage connection is made to the tip with a heavy implant so tip sample biases can be applied independent of the sensor or actuator signals.

Micrographs showing the array of cantilevers with the corresponding bonding pad layout are shown in Fig. 2. We have fabricated an array of 50 cantilevers that are spaced by 200 μm yielding an array spanning one centimeter. Fig. 2a shows the 1 cm array next to a U.S. dime for scale. Fig. 2b shows a detail of five cantilevers within the array. The piezoresistor and ZnO regions are clearly seen. The two horizontal metal lines running across the device are the

piezoresistor and the ZnO ground busses. The three contacts per cantilever (piezoresistor sensor, ZnO actuator, & tip bias) run vertically down the die to the bonding pads shown in Fig. 2d. Each device occupies a horizontal footprint of 200 μm which is the minimum achievable tip to tip spacing due to the design limitations on the bonding pads. (The bonding services currently available to us can bond two rows of pads where each row is on a 100 Rm period. This was the basis for our contact configuration as shown in Fig. 2d.) A close up of the integrated tip is shown in Fig. 2c. The radius of curvature of these single crystal silicon tips is generally less than 100A, This tip was engineered using gas variations in a plasma etch to produce a high aspect ratio profile that is useful for both imaging and lithography. The tips are covered with a thin film of titanium to enhance the capability for lithography.

For small arrays of cantilevers it is possible to manually control all aspects of the cantilever's operation during an imaging or lithography experiment. However, for massively parallel operations, or operation in a scalable system, it is important to have a compact electronic system for automated control. In the piezoresistive/ZnO system, the position of the cantilever arm is detected by microvolt changes in the piezoresistive sensor's bridge circuit. This voltage is amplified to tens of volts to generate a suitable signal for feedback and analysis. Since the voltage gain is high, special considerations need to be given to electronic noise and phase delays in order to create a high speed, sensitive, electronic system. Automation is achieved through computer control of the microscope's operational parameters: force setpoint, gain, and feedback. Two computers are used for imaging. One contains the custom electronic PC expansion board and is responsible for monitoring and modifying the cantilevers operational parameters. The other computer is responsible for collecting data and controlling the scanner.

The transfer function of the electronic system was simulated as the combined electronic and mechanical system. The cantilever was modeled as a second order system with a resonance of 50 kHz and a Q of 100. These parameters were determined from the open loop transfer function of the cantilever when the tip is in contact with a sample. The electronic system was modeled using the written specifications of each of the circuit components. We found excellent agreement between the simulations and the measured data. The primary limitation on bandwidth is due to the resonance of the cantilever. The influence of the electronic phase can be seen in the closed loop response in the small hump before the peak in the amplitude trace. The bandwidth of the amplifier chain is measured to be 1.1 MHz and the phase shift at 100 kHz is less than 10 degrees.

A 32x1 image obtained with the cantilevers and control electronics is shown in Fig. 3. A detail of a memory cell on an integrated circuit chip is shown in Fig. 3a. The ZnO actuator is able to track the 2μm high topography at Imm/s. The minimum detectable deflection for this image is less than 5nm in a 20kHz bandwidth.

III - Fabrication of 100 nm pMOSFETs with Hybrid AFM / STM Lithography

Scanning probe lithography (SPL) where the scanning tunneling microscope (STM) or atomic force microscope (AFM) is used to pattern nanometer-scale features is the foundation of our program. Four factors will dictate the viability of SPL as a patterning technology for the semiconductor industry: 1) resolution, 2) alignment accuracy, 3) reliability, and 4) throughput. We have a new SPL technique-a hybrid between the AFM and STM- to address these issues. We use this to demonstrate the AFM Litho system capability and the compatibility with

semiconductor processing by fabricating a pMOSFET with an effective channel length of 100 nm.

The Hybrid AFM / STM lithography system (as discussed in a following section) combines the key features of the AFM and STM by incorporating two independent feedback loops. One loop keeps the tip on the surface of the resist and maintains a constant force (typically 10 nN). This eliminates the problems of tip penetration into the resist while traveling over topography and minimizes the electron-beam spreading that limits the resolution of STM lithography[10]. The second feedback loop maintains a constant field emission current. Without this feedback loop, any variation in resist thickness (encountered over topography) or any change in tip shape would alter the dose of electrons delivered to the resist.

For the fabrication of this device we used a "mix and match" lithography where the gate level was patterned with Hybrid AFM / STM lithography in air. LOCOS isolation (field oxide = 450 nm) was performed followed by an arsenic channel implant (100 KeV, 1 x 1013 /cm2). The gate oxide thickness was 5.7nm and the polysilicon thickness was 100 nm. Before gate patterning, the poly was implanted with BF2, followed by an RTA (10 sec, N2, 1050°C) to electrically activate the dopants. The poly must be conductive for Hybrid AFM / STM lithography. Low temperature oxide (LTO), 50 nm on thickness, was deposited and patterned by photolithography.

Fig. 4 illustrates the gate patterning steps. Fig. 4a shows the transistor structure after the gate pad formation. A negative-tone e-beam resist (SAL-601) diluted with Microposit Thinner Type A was used. The resist is nominally 60 nm thick after spin on. The resist was first imaged with the AFM in contact mode to precisely locate the position where the gate will be written. The image was then imported into the lithography software, which controlled the path and the speed of the tip. A Ti-coated silicon tip was used to expose the resist (Fig. 4b). After development (Fig 4c), the poly was etched in SF6/Freon 115 plasma where the LTO protects the gate pad and the SAL-601 masks the gate (Fig. 4d).

The resist thickness variation over the LOCOS topography caused by planarization is shown in Fig. 5a and 5b. The thickness changes abruptly from less than 30 nm to more than 90 nm within a micron. The voltage and field-emitted current during exposure are plotted in Fig 5c. The voltage required to maintain 0.05 nA ranges from 22 V to 81 V. Note that a change in voltage, dV/dt, generates a displacement current proportional to the capacitance between the probe and the sample. This parasitic tip-sample capacitance was reduced below 600 fF, which allowed patterning of continuous sub-100-nm features over the 180-nm of topography in a single pass. Fig. 6a was a critical dimension AFM (CD-AFM)[11] image of a 100-nm etched poly feature across the transition region from the field oxide to the active area. The scan speed was 1 μm/s and the line dose was 500 nC/cm .We have fabricated pMOSFETs with a physical gate length ranging from 61 nm to 170 nm.

After gate lithography, a 35 nm oxide spacer was formed by LTO deposition and anisotropic RIE. Shallow source/ drain junctions are created by BF2 implantation (10 KeV, 1x1015/cm2). The final processing steps are: LTO passivation, RTA (10 sec, N2, 1050°C), furnace anneal (30min, N2, 800°C), contact photolithography, metallization, and a forming gas anneal. An optical micrograph of the finished structure was shown in Fig.6b.

This new SPL technique is capable of sub-100-nm resolution and nanometer-scale alignment accuracy with reproducible patterning over significant topography. This system can be extended to high speed and multiple probe patterning and may provide an alternative technology

for critical dimension patterning of 100-nm feature sizes and beyond.

IV - Lithography with Hybrid AFM/STM Probes

We have worked out a new technique for performing lithography with scanning probes that has several advantages over standard methods. This Hybrid AFM / STM lithography system combines the key features of the scanning tunneling microscope (STM) and the atomic force microscope (AFM) by incorporating two independent feedback loops, one to control current and one to control force. We have demonstrated a minimum resolution of 41 nm and alignment capabilities with nanometer precision. This lithography system is capable of writing continuous features over sample topography. Topography is present in real patterning applications and it always poses problems for AFM or STM lithography. We report 100-nm resist features patterned over 180 nm of topography created by LOCOS isolation. The Hybrid AFM/STM is designed as a robust scanning probe lithography system, capable of high-speed patterning and suited for integrated circuit lithography applications.

In scanning probe lithography (SPL) the scanning tunneling microscope (STM) or atomic force microscope(AFM)a voltage bias between a sharp probe tip and a sample generates an intense electric field in the vicinity of the tip. The high field can be used to locally oxidize a variety of surfaces. On silicon, this process is called electric-field-enhanced oxidation[12]. The high field desorbs the hydrogen passivation on the silicon surface, allowing the exposed silicon to oxidize in air (the oxidation rate is enhanced by the presence of the accelerating field). These oxidation processes are powerful because of the fine resolution and the resistant oxide etch mask that is created. Patterning is slow, however, limited by the reaction rate at the surface. Writing speeds are typically under 10 μm/s, making patterning of finite areas in reasonable times unmanageable[13]. Local oxidation also results in significant tip wear[14].

Another system for performing lithography with scanning probes involves the electron exposure of a resist material, such as an organic polymer or a monolayer resist. When a conducting tip is biased negatively with respect to a sample, electrons are field-emitted from the tip. If as sample is coated with a thin resist, the emitted electrons traverse the resist. The resist absorbs energy from the electrons and this induces chemical changes in the resist. The resist pattern can then be transferred to the substrate using selective chemical etching or dry etching. Organic polymer resists provide an attractive option for SPL because they have a low threshold voltage, high sensitivity, sub-100-nm resolution, and good dry etch resistance. Moreover, these resists can be easily deposited on virtually any substrate, and most organic polymers are well characterized from their use in photolithography or electron beam(e-beam) lithography. It is also possible to pattern at higher speeds with this method. Finally, the polymer surface is soft and pliable which should significantly reduce the tip wear .

We have developed a lithography system, a hybrid between the AFM and STM, which is capable of patterning sub-100-nm features on a variety of substrates, with various tips, and over topography. It requires minimal characterization prior to patterning and is designed for high speed lithography and the extension to multiple probes arrays simultaneously. In STM lithography, a fixed tip-sample bias is applied and the spacing is varied to maintain a constant current through the resist. This system suffers from poor alignment capabilities (imaging may expose the resist). The appropriate voltage bias for STM lithography is tricky. If the bias is set too high, the tip may

move far from the sample resulting in beam spreading. If the bias is too low, the tip may in fact penetrate the resist in an attempt to achieve the setpoint current. In AFM lithography, the force between the tip and resist is held constant while a fixed voltage bias is applied to generate the field-emitted current. Constant-voltage operation is not ideal since the required voltage is a function of the tip and sample materials, the tip shape, and the resist thickness. Therefore, a change in tip shape or resist thickness will vary the dose of electrons delivered to the resist and produce non-uniform patterns.

Our system combines the key features of the AFM and STM by incorporating two independent feedback loops (Fig. 7a). One loop keeps the tip on the surface of the electron-sensitive resist and maintains a constant small force between the tip and sample (typically 10 nN). This minimizes the beam spreading that limits the resolution of STM lithography. The second feedback loop maintains a constant field emission current through the resist during exposure (generally in the range of 20 pA to 1nA). This custom-built analog feedback circuit, shown in Fig. 7b, uses integral gain to minimize the current error signal. The feedback circuit compares the measured current to the setpoint current. A high voltage amplifier applies the necessary voltage to the sample (generally 20-100 V) to maintain the setpoint current.

We have demonstrated Hybrid AFM / STM lithography by patterning Microposit SAL-601. SAL-601 is a chemically-amplified resist (CAR), which makes it highly sensitive to electron exposure. The high resolution of SAL-601 has been previously demonstrated with x-ray, e-beam, and STM lithography. We patterned SAL-601 resist on various substrates: phosphorus-doped silicon and boron-doped polysilicon. The sample preparation steps are listed in Table 1. Before resist coating, the native oxide was etched off the substrate in 50:1 hydrofluoric acid (HF). The substrates were then singed for 30 minutes in a 150°C convection oven and vapor primed with hexamethyldisilazane (HMDS) adhesion promoter. SAL-601diluted in Microposit Thinner Type A was spin coated on the wafer. The wafer was prebaked (1 min, 85°C hotplate followed by 30 min, 90°C convection oven).

Exposure was performed in air using the PSI Autoprobe M5 operating in contact AFM mode as modified with constant-current feedback circuitry. We used high-aspect-ratio doped-silicon tips, some of which were coated with 20 nm of evaporated titanium (Ti), tantalum (Ta), or molybdenum(Mo). With the Ti coating, the tip radius is approximately 30-40 nm. We were careful to minimize the tip-sample capacitance. This capacitance becomes important when attempting to maintain constant current at high speeds or over topography (where the voltage must change rapidly).

The resist and etched lines were characterized using: 1) a 100Xmagnification optical microscope for preliminary inspection; 2) the AFM operating in noncontact mode to determine line continuity and uniformity; and 3) the Dektak SXM critical dimension AFM (CD-AFM) for measuring linewidths. Noncontact mode AFM operation was adopted for line continuity and uniformity inspection. Contact mode operation was not acceptable since the scanning tended to damage the resist lines. The Dektak CD-AFM was operated in a two-dimensional noncontact scanning mode using a boot shaped tip[15]. The tip shape is optimized to sense topography on vertical surfaces and can be used to profile vertical or even re-entrant sidewalls (where conventional conical or pyramidal tips fail as a result of tip-sample convolution). The resolution of the CD-AFM is approximately 50 Å laterally. Previous studies have shown that CD-AFM

linewidth and profile measurements correlate well with cross section scanning electron microscope (SEM) data[16]. An advantage of the CD-AFM is that it is capable of making these measurements non-destructively (without cleaving the wafer and preparing across section), and measurements and images can be obtained anywhere on the wafer (not just where the cross section was made).

The Hybrid AFM / STM system allows us to measure the field emission characteristics of the tip-resist-substrate system by varying the setpoint current and measuring the applied voltage. Once the field becomes high enough for current to flow (above this 21 volt "threshold"), the current increases dramatically with voltage. This I-V relationship depends critically on the tip shape and the resist thickness. A more blunt tip would require a higher bias to reach the critical field for electron emission. Fowler and Nordheim predicted an exponential dependence of the field-emitted current on the bias voltage[17]. Data does indeed indicate an extreme sensitivity of current on bias voltage, but the behavior is not exponential.

Resolution and Throughput

We have studied the line width of the developed resist and its dependence on line dose. From this data we conclude that the critical parameter for exposing an organic polymer with scanning probes is the dose of electrons delivered to the resist. In the case of SPL, the line dose (in Coulombs/cm) is the ratio of the current to the writing speed. The width of the exposed region depends critically on this line dose. Features can be patterned at higher speeds by increasing the current proportionally. Because of the current sensitivity on voltage, current can be increased by orders of magnitude with only a few volts change. Therefore this patterning technique can be extended to higher speed lithography. We have patterned at speeds up to 200 μm/s and foresee no physical speed limitations to this patterning mechanism within reasonable scan speeds. The smallest lines we have patterned are 41 nm at a line dose of 26 nC/cm.

Patterning Over Topography

Patterning over topography is a challenge for most forms of lithography. Resist spun on a wafer with topography tends to planarize, resulting in thickness variations across the sample. It is difficult to achieve uniform patterns over topography using e-beam lithography. This is a result of electrons backscattering from the substrate and changing the feature profile near a topographic step. For different reasons, it is impractical to pattern a wafer with topography with the standard STM or AFM. In STM lithography the problem is usually one of beam spreading causing linewidth variations between regions. A more aggressive attempt to limit beam spreading can cause the tip to penetrate the resist in the thicker regions. With the AFM, a given bias will likely pattern only one region (perhaps the thinner resist), but not expose another region at all. The Hybrid AFM/STM lithography system was designed to circumvent these problems.

The Hybrid AFM/STM system delivers a constant dose of electrons while maintaining a minimum tip-sample spacing. This allows patterning of continuous and uniform features over topography.

A change in voltage, dV/dt, generates a displacement current proportional to the capacitance between the probe and sample. The total current measured is thus a sum of the d.c. current through the resist and this capacitive current. If a significant fraction of the total current is

capacitive, the dose of electrons delivered to the resist is not constant. In particular, whenever the voltage changes abruptly, there can be a break in the exposure. We measured the probe-sample capacitance as about 2.4 pF. We estimate a contribution to the total capacitance of less than $1x10^{-18}$ F from the tip itself (modeling the tip as a sphere). The cantilever, although quite close to the sample, is small in area (about $1x10^4$ μm^2) and therefore contributes only a few fF.

The Hybrid AFM/STM system is a robust lithographic tool, capable of patterning a variety of materials, resists, and topography by simply setting the desired exposure dose. Constant force operation enables fine resolution lithography by minimizing beam spreading. Constant current operation delivers a fixed dose of electrons to the resist allowing reproducible and uniform lithography. Alignment accuracy of a few nanometers is possible with the Hybrid AFM / STM system because the underlying layer is first imaged in AFM mode. Electron dose is found to be the critical exposure parameter. Because of the sensitivity of field-emission current on voltage bias, writing speeds may be dramatically increased with only small changes in the voltage. Since the bias for field-emission is less than 100 V, proximity effects often found in high energy-beam lithography should be minimal.

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FIGURE CAPTIONS

Figure 1. Schematic illustration of the expandable cantilever design with integrated piezoresistive sensor and integrated ZnO actuator. The perspective view on the left shows the final device, while the exploded view on the right shows the pattern of all of the films in the device.

Figure 2. An array of cantilevers with integrated actuators and sensors with improved shielding between the actuator and sensor. Part (a) shows an entire array of 50 cantilevers spanning I cm next to a U.S. dime (for scale). In (b) we show a detail of five of the cantilevers. The cantilevers are spaced by 200 gm c) SEM of a typical integrated single crystal silicon tip. The radius of curvature is below l0nm d) corresponding electrical contact structure for the cantilevers. There are three leads per device: piezoresistor, ZnO and tip bias.

Figure 3. 32x1 images of a memory cell of an integrated circuit obtained in parallel with the cantilevers shown in Figure 2. The bandwidth of the system in 20 kHz, and the sensitivity is less than 5 nm in that band.

Figure 4. Schematic of the gate patterning procedure; a) LTO gate pad is photolithographically defined; b) SAL-601 resist is spun and Hybrid AFM/STM lithography is performed; c) Exposed gate remains after development; d) Poly is etched by RIE.

Figure 5. a) Poly and resist topography created by LOCOS isolation. b) Resist thickness variation as a function of position; c) Current and voltage during Hybrid AFM/STM lithography.

Figure 6. CD-AFM image of an etched 100 nm polysilicon feature over 180 nm of topography created by LOCOS isolation. The line was patterned with a line dose of 500 nC/cm.

Figure 7. a.) Schematic diagram of the Hybrid AFM/STM lithography system incorporating dual feedback loops, one to maintain a constant force between the tip and sample and the other to keep a constant field-emission current through the resist. b.) Schematic diagram of the integral current feedback circuit, which changes the sample bias in order maintain the setpoint current.

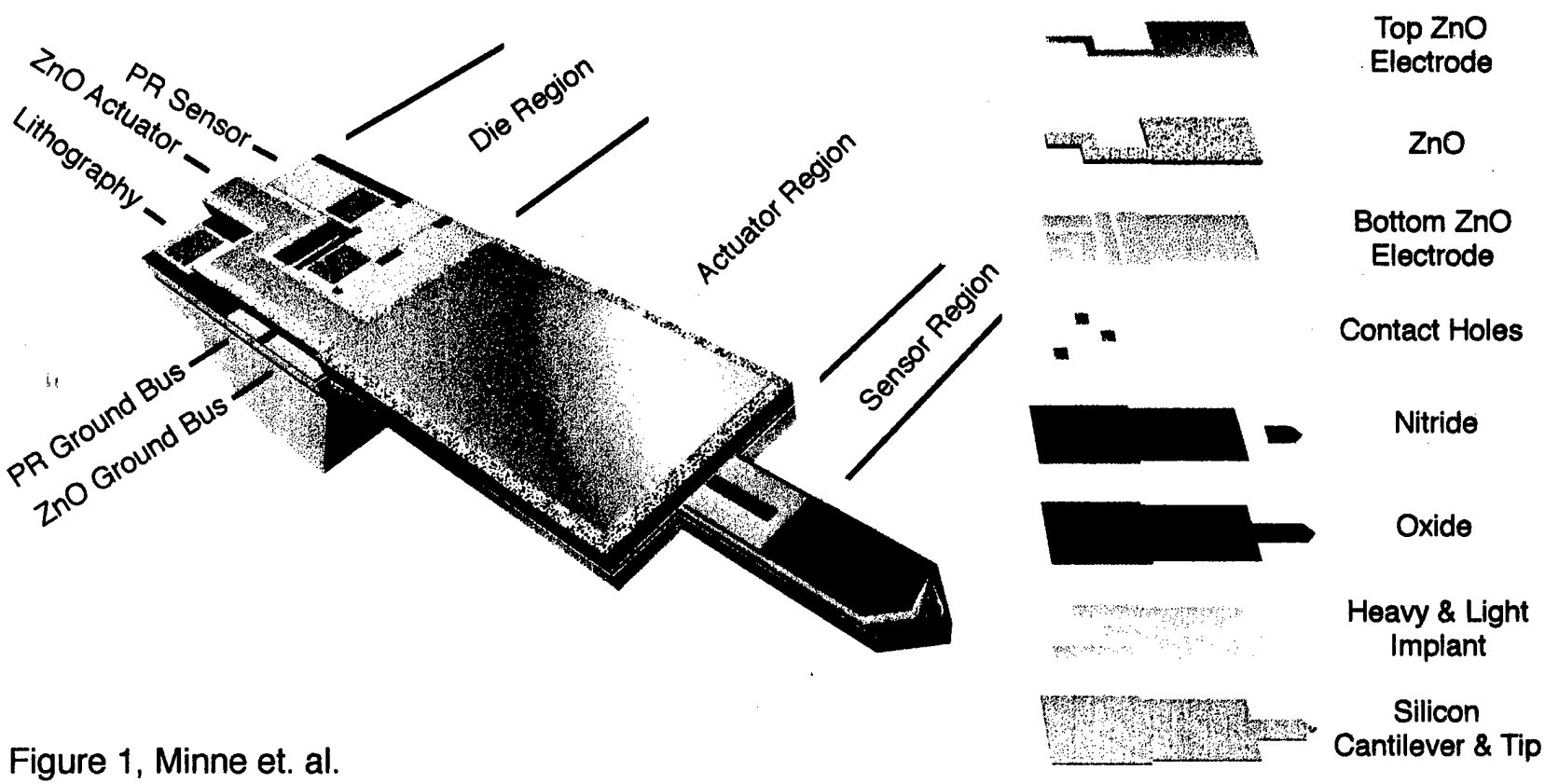
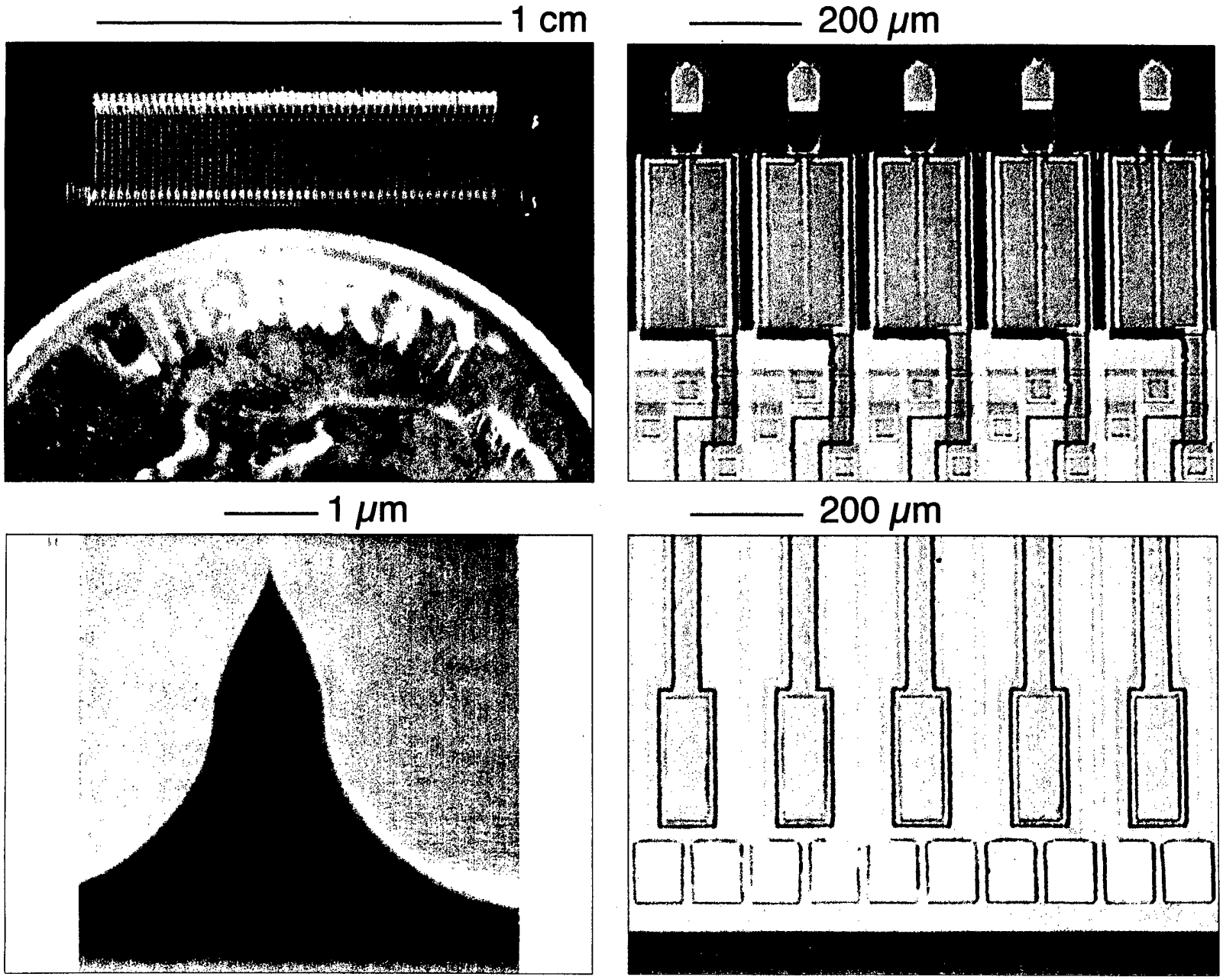


Figure 1, Minne et. al.



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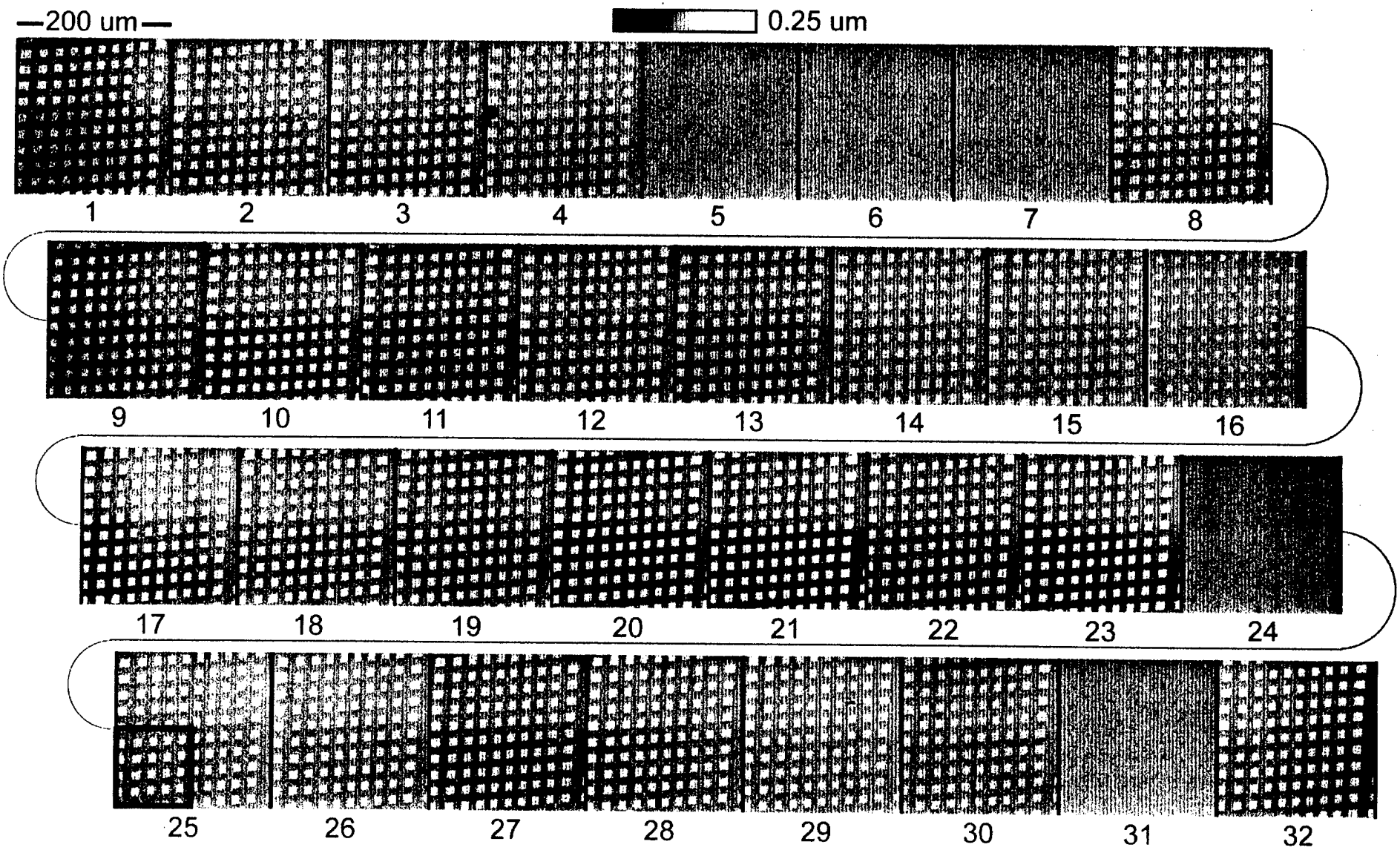

Figure 2, Minne et. al.

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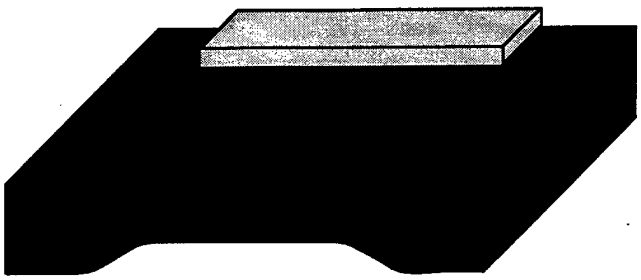

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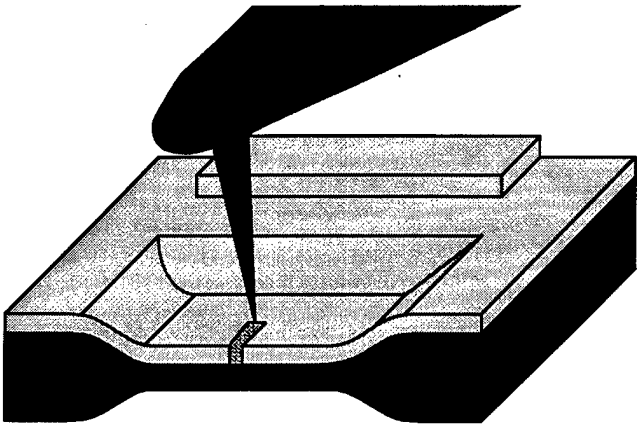

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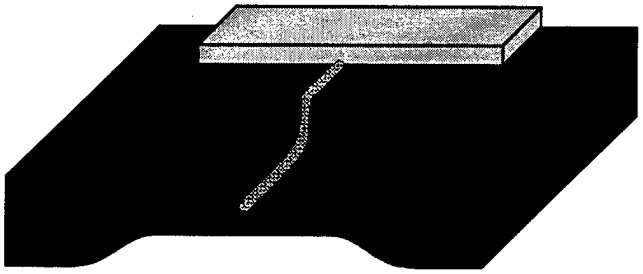

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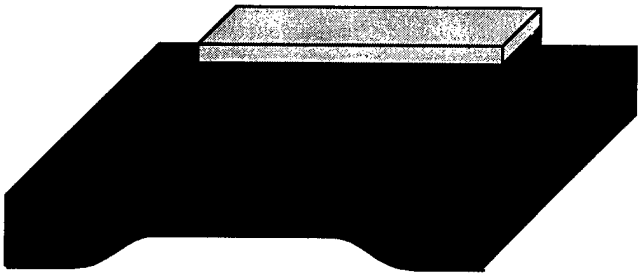


Figure 4

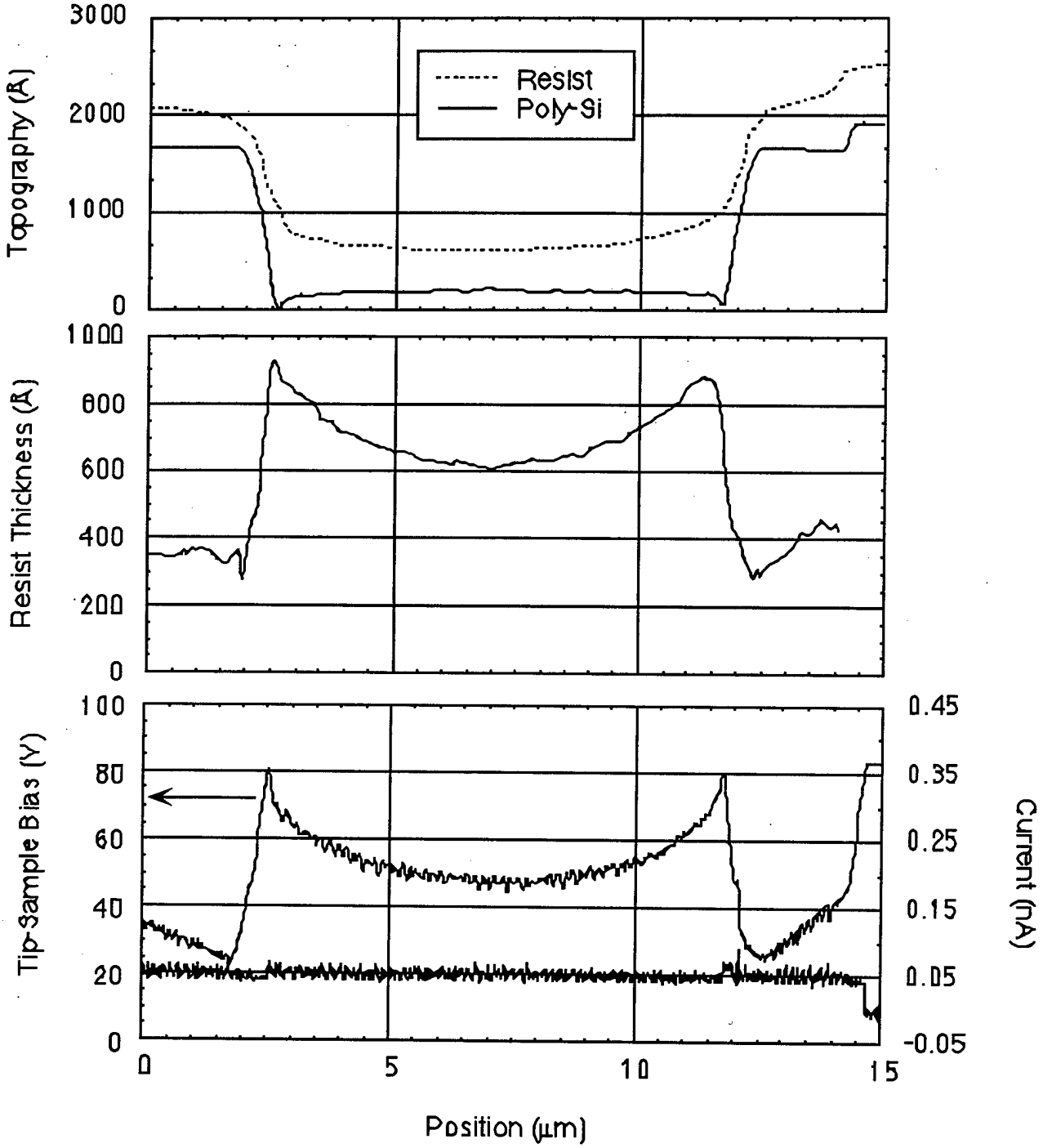

Topography (Å)
3000
2000
1000
0
Resist
Poly-Si
Resist Thickness (Å)
1000
800
600
400
200
0
Tip-Sample Bias (V)
100
80
60
40
20
0
Current (nA)
0.45
0.35
0.25
0.15
0.05
-0.05
0
5
10
15
Position (µm)

Figure 5

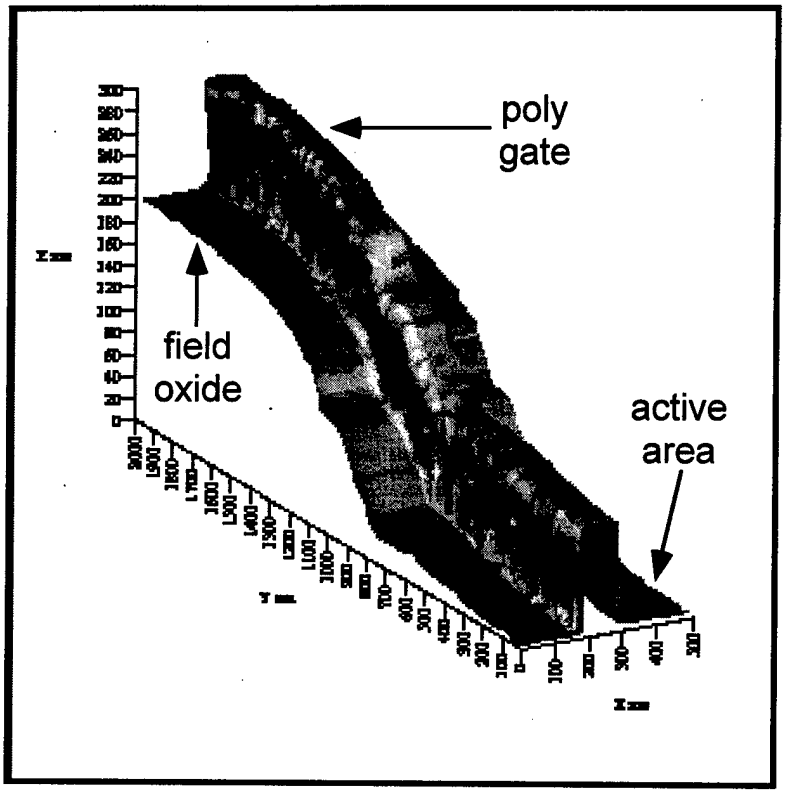
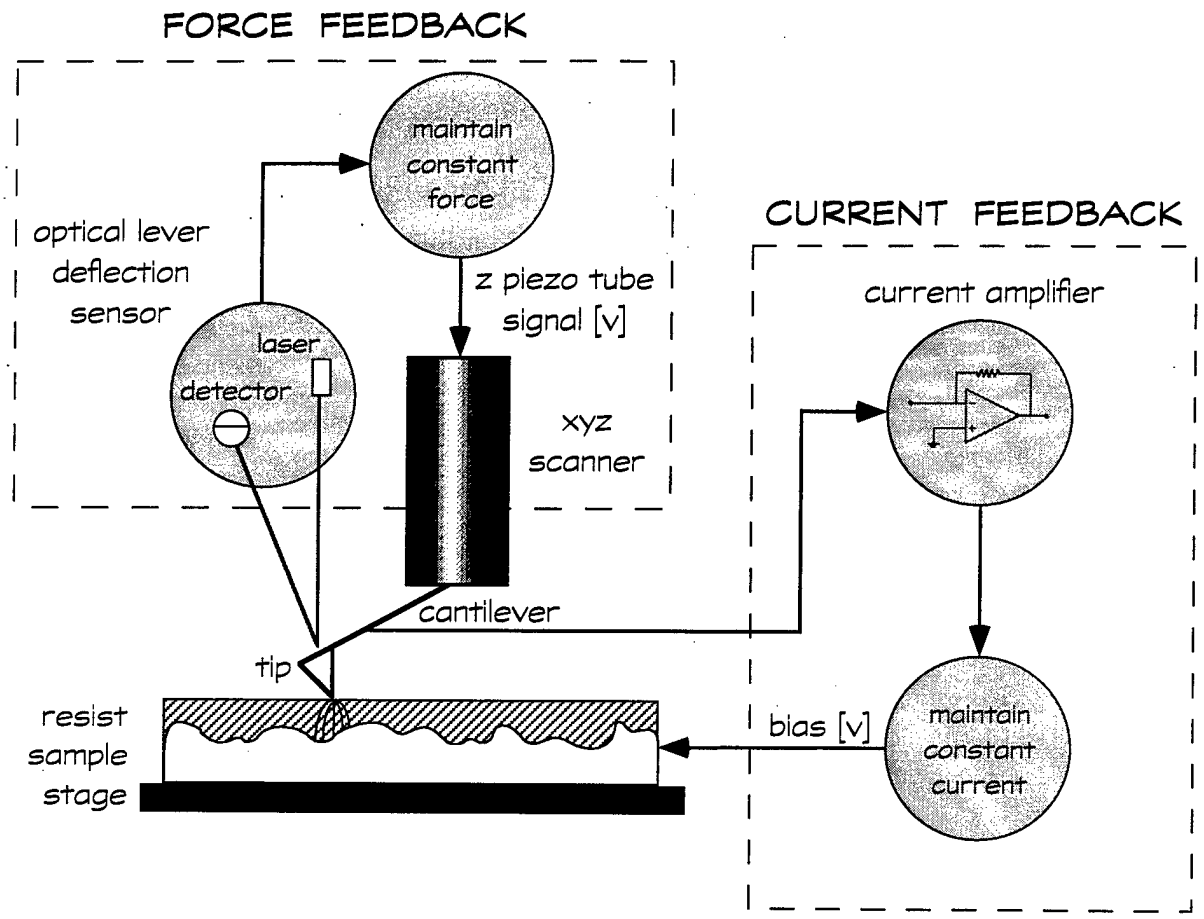


Figure 6

a)


FORCE FEEDBACK
maintain constant force
optical lever deflection sensor
z piezo tube signal [v]
laser detector
xyz scanner
CURRENT FEEDBACK
current amplifier
cantilever
tip
resist sample stage
bias [v]
maintain constant current

b)

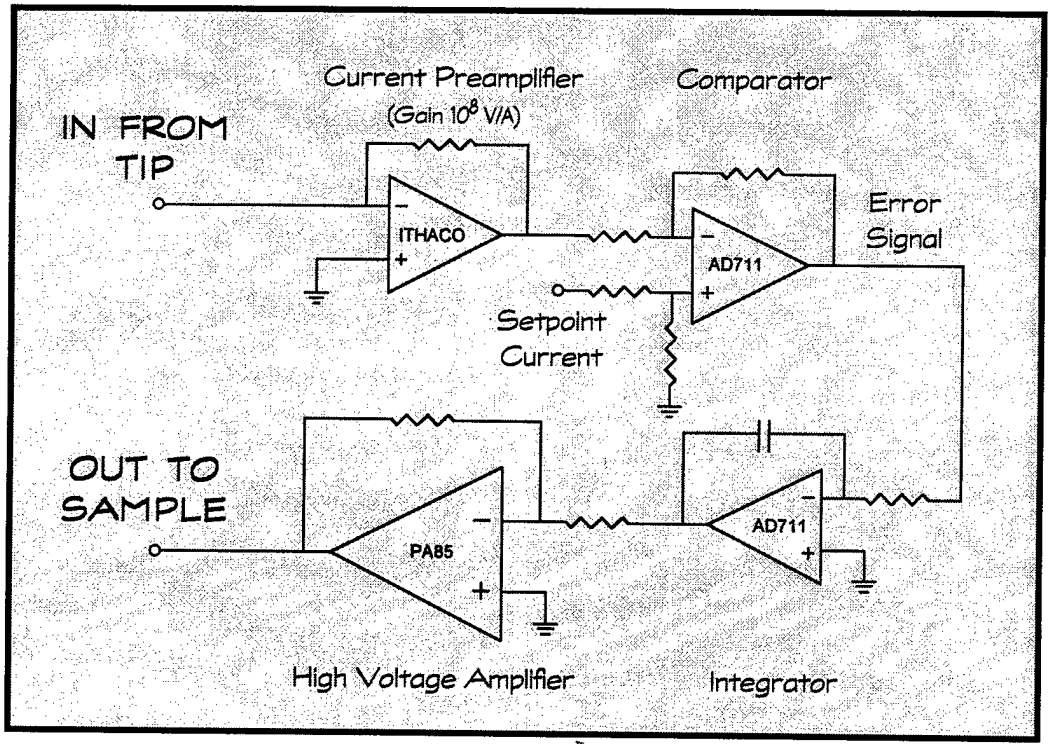

Current Preamplifier
(Gain 10^8 V/A)
Comparator
IN FROM TIP
ITHACO
AD711
Error Signal
Setpoint Current
OUT TO SAMPLE
PA85
AD711
High Voltage Amplifier
Integrator

Figure 7

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REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	April 7, 1998	Annual - 1 January 1997 - 31 December 97

4. TITLE AND SUBTITLE
Sub-Micron Lithography with the Atomic Force Microscope

5. FUNDING NUMBERS
N00014-96-1-0771

6. AUTHOR(S)
Calvin Quate and Steve Minne

7. PERFORMING ORGANIZATION NAMES(S) AND ADDRESS(ES)
Calvin F. Quate
Department of Electrical Engineering
Stanford University
Ginzton Laboratory, Room 12
Stanford, CA 94305-4085

8. PERFORMING ORGANIZATION REPORT NUMBER
96PR05481-00

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Office of Naval Research
Program Officer Richard G. Brandt ONR 312
Ballston Centre Tower One
800 North Quincy Street
Arlington, VA 22217-5660

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*
See attached report.

14. SUBJECT TERMS

15. NUMBER IF PAGES
19

16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL